Question Paper - Report

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Question Paper

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MANIPAL ACADEMY OF HIGHER EDUCATION

BTech II Semester MIDSEM Examination March 2025

FUNDAMENTALS OF ELECTRONICS [ECE 1072-PHY]

Marks: 30 **Duration: 90 mins.**

MCQ

Answer all the questions. Section Duration: 20 mins

1) Which of the following statement is FALSE? (1)

Ideal value of Open loop voltage gain of OP-AMP is Infinity. | Ideal value of output resistance of OP-AMP is Zero. | Ideal value of bias current of OP-AMP is Infinity. | Ideal value of CMRR of OP-AMP is Infinity.

2) For the circuit shown below, the output voltage V_O is ----------. Assume D1, D2, and D3 as germanium diodes (1)

1 V | 0.7 V | 0.3 V | 0 V

3) For the circuit shown, the output voltage V_O is ---------. Assume D1 to be Ge diode, D2 to be ideal diodes. (1)

1 V | 0.3 V | 0.7 V | 0 V

4) For the given circuit, the output voltage V_{OUT} is --------- (1)

−12V | 20Sin(wt) | +12V | None of these

5) For the given circuit, the value of resistance RL is ------- to obtain an output of 2V (1)

10 Ω | 1K Ω | 100 Ω | 20 Ω

Descriptive

Answer all the questions.

6) Obtain an expression for drain current of MOSFET in terms of gate to source voltage, drain to source voltage and W/L. Also, sketch V_{DS} - I_D Characteristics and mark the various region of operation. For the circuit shown in the figure, find the region of operation of MOSFET. Assume $\mu_n C_{OX}$ = 200μA/V^2 , V_{TH} =0.5V (4)

7) (3)

8) Determine the range of R_L to obtain a regulated output voltage of 10V in the circuit shown below. Assume V_{IN} = 12V, R=10Ω, the maximum power rating of Zener diode and minimum value of Zener current as 1W and 0.2mA. (3)

9) For the circuit shown in the figure, assuming an ideal diode, determine
(a) DC output voltage
(b) Rectifier efficiency
(c) Peak inverse voltage
(d) DC Output voltage, if a capacitor of 1mF is connected across 1KΩ load resistance.
(e) RMS output current
(f) Output frequency (3)

10) Design the circuit using two OPAMPs such that output voltage is given by $Vo = V_1 - 5\ V_2 - 3\ V_3$, where V_1, V_2, V_3 are inputs to the OPAMP. Assume feedback resistance as 10KΩ (3)

11) For the circuit shown in figure, determine the maximum allowable value of W/L for a drain resistance (R_D) of 3KΩ that can maintain M1 in saturation region. Assume V_{TH} = 0.4V, $\mu_n C_{ox}$ = 100 μA/V^2. (3)

12) Consider an OP-AMP that gives an output voltage of 10V with input voltages V1= 1mV and V2 = - 1mV. If the same OP-AMP gives an output voltage of 5mV for V1 = 0.5mV and V2 = 0.5mV, determine the CMRR of OP- AMP. (2)

13) Design a circuit using an OP-AMP to obtain a voltage gain of -10. Assume the feedback resistance value as 10KΩ. (2)

14) In the circuit shown, find the DC Current through 1KΩ resistance for an input voltage of V_{IN} = (5 sin(wt) + 5) Volts (2)